AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A processing device comprising:

one or more resources within a node;

a plurality of peripheral bus interfaces ~~operably~~ coupled to the one or more resources and ~~to couple~~ coupled to a peripheral bus fabric to support resource sharing with a plurality of other processing devices of other nodes when the other processing devices are coupled to the peripheral bus fabric;

a node identification (ID) register ~~programmable to have~~ including primary routing resources programmable with a plurality of addresses to determine a primary routing of a peripheral bus transaction among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction ~~and a particular type of transaction~~; and

the node ID register also ~~to have~~ including a node routing table containing one or more override indications to determine ~~an~~ one or more alternate override routing of the peripheral bus transaction ~~among the plurality of peripheral bus interfaces~~ over the primary routing and, in which the primary routing for the peripheral bus transaction is overridden by one or more alternate override routing when the destination address and a type of transaction for the peripheral bus transaction is indicated by one or more override indications in the node routing table ~~based upon the destination address and when a type of transaction is other than the particular type of transaction noted for the primary routing~~.

2. (currently amended) The processing device of claim 1 wherein the processing device determines a node ID of a destination ~~processing~~ device based upon a set of most

significant bits of the destination address of the peripheral bus transaction.

3. (previously presented) The processing device of claim 1 wherein the processing device is to ignore the alternate override routing based upon programmed contents of the node ID register.

4. (currently amended) The processing device of claim 1 wherein ~~the~~ one alternate override routing indication applies to the peripheral bus transaction when the peripheral bus transaction is a cache coherency peripheral bus ~~transactions~~ transaction.

5. (currently amended) The processing device of claim 1 wherein ~~the~~ one alternate override routing indication applies to the peripheral bus transaction when the peripheral bus transaction is an input/output peripheral bus ~~transactions~~ transaction.

6. (currently amended) The processing device of claim 1 wherein ~~the~~ a first alternate override routing indication applies to the peripheral bus transaction when the peripheral bus transaction is a ~~to both~~ cache coherency peripheral bus transactions and ~~to~~ a second alternate override routing indication applies to the peripheral bus transaction when the peripheral bus transaction is an input/output peripheral bus ~~transactions~~ transaction.

7. (currently amended) The processing device of claim 6, wherein the alternate override routing is selectively disabled with regard to cache coherency peripheral bus transactions and/or ~~to~~ input/output peripheral bus transactions~~, in which an override disabled transaction is to use the primary routing~~.

8. (previously presented) The processing device of claim 6 wherein a packet data peripheral bus transaction is designated for primary routing.

9. (currently amended) The processing device of claim 1, ~~wherein:~~ wherein each of the override ~~routing~~ indications also indicates ~~to route the peripheral bus transaction to~~ either a primary port ~~of an override selected peripheral bus interface or to~~ or a secondary port of ~~the override selected~~ one of the peripheral bus interfaces selected for override routing of the peripheral bus transaction.

10. (currently amended) The processing device of claim 1 wherein the node ~~ID register comprises~~ routing table includes an entry for each of a plurality of ~~represented~~ processing devices, each entry comprising:

an override bit corresponding to input/output peripheral bus transactions;

a primary/secondary port indication corresponding to input/output peripheral bus transactions;

an override bit corresponding to cache coherency peripheral bus transactions; and

a primary/secondary port indication corresponding to cache coherency peripheral bus transactions.

11-28. (canceled)

29. (currently amended) A method for operating a processing device having one or more resources and a plurality of peripheral bus interfaces that are operable to couple the one or more resources of a node to one or more other processing devices of other nodes via a peripheral bus fabric, the method comprising:

receiving a peripheral bus transaction at the processing device;

determining a primary routing of the peripheral bus transaction among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction ~~and a particular type of transaction~~ programmed in a node identification (ID) register;

determining an alternate override routing of the peripheral bus transaction among the plurality of peripheral bus interfaces based upon ~~the address and when a type of transaction is other than the particular type of transaction noted for the primary routing, the override routing also programmed in the node ID register~~ entries in a node routing table, in which the primary routing for the peripheral bus transaction is overridden by an alternate override routing when the destination address and a type of transaction for the

peripheral bus transaction is indicated by an override indication in the node routing table; and

routing the peripheral bus transaction among the plurality of peripheral bus interfaces ~~using different paths~~ according to the primary routing, unless the node routing table indicates an entry to override the primary routing ~~or the override routing~~ based on the type of transaction ~~noted~~ for the peripheral bus transaction.

30. (currently amended) The ~~processing device~~ method of claim 29 further comprising determining a node ID of a destination ~~processing~~ device based upon a set of most significant bits of the destination address of the peripheral bus transaction.

31. (canceled)

32. (currently amended) The method of claim 29 further comprising applying the alternate override routing to the peripheral bus transaction when the peripheral bus transaction is a cache coherency peripheral bus ~~transactions~~ transaction.

33. (currently amended) The method of claim 29 further comprising applying the alternate override routing to the peripheral bus transaction when the peripheral bus transaction is an input/output peripheral bus ~~transactions~~ transaction.

34. (currently amended) The method of claim 29 further comprising applying the alternate override routing to ~~both~~ the peripheral bus transaction when the peripheral bus transaction is either a cache coherency peripheral bus ~~transactions and to~~ transaction or an input/output peripheral bus ~~transactions~~ transaction.

35. (previously presented) The method of claim 34, further comprising applying the primary routing to a packet data peripheral bus transaction.